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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
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| 09/510,375 | 02/22/00 | WILLIAMS | B 303.164US3 |

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| EXAMINER | |
|---|---|
| KIM, H | |
| **ART UNIT** | **PAPER NUMBER** |
| 2185 | 4 |

**DATE MAILED:** 12/29/00

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

| Office Action Summary | Application No. 09/510,375 | Applicant(s) Williams |
|---|---|---|
| | Examiner H. Kim | Group Art Unit 2185 |

*—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—*

**Period for Response**

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 (three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

**Status**

☒ Responsive to communication(s) filed on 2/22/00.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

**Disposition of Claims**

☒ Claim(s) 26-37 is/are pending in the application.

Of the above claim(s) 1-25 is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 26-37 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

**Application Papers**

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☒ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119 (a)-(d)**

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received: _____.

**Attachment(s)**

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 2

☒ Notice of References Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

**Office Action Summary**

**Detailed Action**

1. Claims 26-37 are presented for examination. This office action is in response to the application filed on 2/22/00. Claims 1-25 have been canceled by the amendment.

2. This application repeats a substantial portion of prior Application No. 08/386,894 filed February 10, 1995, now U.S. Patent No. 5,610,864, which is a continuation-in-part of U.S. Serial No. 08/370,761 filed December 23, 1994, now U.S. Patent No. 5,526,320 and adds and claims additional disclosure not presented in the prior application. Should applicant desire to obtain the benefit of the filing date of the prior application, attention is directed to 35 U.S.C. 120 and 37 CFR 1.78. It is unclear to the Examiner how the prior Application No. 08/386,894 can be obtained the benefit of the filing data since there is no common inventor(s) in the prior Application No. 08/386,894. Applicant is requested to clearly point out which limitation is continuation and CIP in order to obtain the benefit of the filing data.

3. Receipt is acknowledged of information disclosure statement filed on 2/22/00, which the statement has been placed of record in the file. Information disclosed and listed on PTO 1449 was considered.

*Specification*

4. The title of the invention is not descriptive. A new title is required that is clearly indicative

of the invention to which the claims are directed. The title should be more specific to differentiate the invention from similar inventions in the patent literature. The "burst extended data out", "fast page mode", and "power detection" aspects of the invention should be mentioned in the title so that the title is more descriptive.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. Claim 37 is rejected under 35 U.S.C. 102(a) as being anticipated by Tanaka et al. (Tanaka) US Patent No. 5,325,513.

As to claim 37, *Tanaka* discloses the invention as claimed. *Tanaka* discloses a system, comprising:

a memory controller (Fig. 1 Ref. 110 and Fig. 2 Ref. 13's); and

a memory (Fig. 1 and Fig. 2 Refs. 20's), wherein the memory comprises: a first bank (Fig. 1 Ref. 20a) and a second bank (Fig. 1 Ref 20b), wherein the first bank and the second bank are each independently interchangeably of a memory type (independent timing signal generator Ref 13 reads on this limitation since any memory can be placed on Refs 20's) selected from the group consisting of a first type of memory and a second type of memory, further wherein the memory

controller controls access of the first bank and second bank in accordance with a first set of requirements for the first type of memory and a second set of requirements for the second type of memory.

### *Claim Rejections - 35 USC § 103*

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 34 is rejected under 35 U.S.C. 103(a) as being anticipated by Farrer et al. (Farrer) US Patent No. 5,307,320 in view of Fung et al. (Fung) US Patent No. 5,630,163.

As to claim 34, *Farrer* discloses a system, comprising:

a bus for transferring information (Fig. 1 Ref. 105);

a memory (Fig. 1 Ref. 103), coupled to the bus, comprised of a memory device having a first operation mode (Fig. 3 Ref. 301) and a second operation mode (Fig. 3 Ref. 302), wherein the memory has a first set of access control signals for operation in the first operation mode and a second set of access control signals for operation in the second operation mode;

a programmable memory controller (col. 5 lines 16 and 54-66), coupled to the bus and to the memory, capable of providing the first set of access control signals and the second set of access control signals to the memory;

a processor (Fig. 1 Ref. 101), coupled to the bus and the memory controller wherein the processor is responsive to at least information from the memory to program the memory controller to provide the first set of access control signals to the memory at a first time and the second set of access control signals to the memory at a second time.(col. 5 lines 50-66).

However, Farrer does not specifically disclose a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller; wherein the processor is responsive to at least information from the memory to program the memory controller to provide the first set of access control signals to the memory at a first time and the second set of access control signals to the memory at a second time.

Fung disclose a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller (col. 1 lines 25-32, BIOS read on this limitation since the BIOS operates during a power up routine) for the purpose of determining a computer configuration thereby guaranteeing reliable operation of the system. Also it would have been readily appreciated by one of ordinary skill in the art that a system includes a power supply to provide a power to the system.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the power supply and a power up detection circuit coupled to the

processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller of Fung into the invention of Farrer for the advantages stated above.

9. Claims 35-36 are rejected under 35 U.S.C. 103(a) as being anticipated by Tanaka et al. (Tanaka) US Patent No. 5,325,513 in view of Wyland US Patent No. 5,261,064 and further in view of Micron, "Reduce DRAM cycle times with extended data-out", Micron technical Note pp 5-33 thru 5-40, 4/94.

As to claim 35, *Tanaka* discloses a system, comprising:

a memory controller (Fig. 1 Ref. 110 and Fig. 2 Ref. 13's); and

a memory (Fig. 1 and Fig. 2 Refs. 20's), wherein the memory comprises:

a first bank of memory (Fig. 1 Ref 20a) coupled to the memory controller to receive a plurality of access control signals; and

a second bank (Fig. 1 Ref 20b) comprised of a memory type selected from the group of memories (col. 1 lines 38-40), wherein the second bank is coupled to the memory controller to receive the plurality of access control signals, further wherein the memory controller drives the access control signals in a first mode to provide access to the first bank, still further wherein the memory controller drives the access control signals in a second mode to provide access to the second bank.

Although Tanaka discloses different types of memories, Tanaka doses not specifically disclose a

first bank of burst access memory coupled to the memory controller.

However it is well known in the memory art a memory can be operate in a burst mode. For example Wyland discloses burst mode of operation (abstract lines 2-3) in order to increase access time (col. 1 lines 15-16).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use burst access memory of Wyland in the invention of Tanaka for the purpose of increasing access time thereby increasing overall system performance.

Furthermore, neither Tanaka nor Wyland discloses a second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory.

Micron discloses the second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory (page 5-33 bottom of right column and page 5-39 bottom of right column) thereby the user may base the design of the computer system on the type of memory that offers the target price/performance ration of the system.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory of Micron in the combined invention of Tanaka and Wyland for the advantages stated above.

As to claim 36, *Tanaka* further discloses the system of claim 35, wherein the memory

type of the second bank is interchangeable (independent timing signal generator Ref 13 reads on this limitation since any memory can be placed on Refs 20's). *Micron* further discloses the system of claim 35, wherein the memory type of the second bank is interchangeable (page 5-33 bottom of right column and page 5-39 bottom of right column).

10. Claims 26, 29 and 32 are rejected under 35 U.S.C. 103(a) as being anticipated by Farrer et al. (Farrer) US Patent No. 5,307,320 in view of Micron, "Reduce DRAM cycle times with extended data-out", Micron technical Note pp 5-33 thru 5-40, 4/94 and further in view of Wyland US Patent No. 5,261,064.

As to claims 26, 29, and 32 *Farrer* discloses a system, comprising:

a bus (Fig. 1 Ref. 105) for transferring information;

a memory (Fig. 1 Ref. 103), coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of a first mode (Fig. 3 Ref. 301) and a second mode (Fig. 3 Ref. 302), the memory having a first set of access control signal timing requirements for the first mode and a second set of access control signal timing requirements for the second mode;

a programmable memory controller (col. 5 lines 16 and 54-66), coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory; and

a processor (Fig. 1 Ref. 101), coupled to the bus and the memory controller, responsive to at least

information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

However Farrer does not specifically disclose a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the extended data out mode and a second set of access control signal timing requirements for the fast page mode.

Micron discloses a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the extended data out mode and a second set of access control signal timing requirements for the fast page mode (page 5-33 bottom of right column and page 5-39 bottom of right column) thereby the user may base the design of the computer system on the type of memory that offers the target price/performance ration of the system. *Micron* further discloses that the memory device is interchangeable (page 5-33 bottom of right column and page 5-39 bottom of right column).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of extended data out mode and fast page mode, the memory having a first set of access control signal timing

requirements for the extended data out mode and a second set of access control signal timing requirements for the fast page mode of Micron in the invention of Farrer for the advantages stated above.

Furthermore neither Farrer nor Micron discloses a burst mode.

However it is well known in the memory art a memory can be operate in a burst mode. For example Wyland discloses burst mode of operation (abstract lines 2-3) in order to increase access time (col. 1 lines 15-16).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use burst access memory of Wyland in the combined invention of Farrer and Wyland for the purpose of increasing access time thereby increasing overall system performance.

11. Claims 27-28, 30-31, and 33 are rejected under 35 U.S.C. 103(a) as being anticipated by Farrer et al. (Farrer) US Patent No. 5,307,320 Micron Reduce DRAM cycle times with extended data-out, Micron technical Note pp 5-33 thru 5-40, 4/94 and Wyland US Patent No. 5,261,064 and further in view of Fung et al. (Fung) US Patent No. 5,630,163.

As to claims 27-28, 30-31, and 33, *Farrer, Micron, ,and Wyland* disclose the invention substantially as claimed in the above claim. However, neither Farrer, Micron, nor Wyland specifically discloses a power supply; and a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power

supply to cause the processor to detect the memory device mode and to program the memory controller; wherein the processor is responsive to at least information from the memory to program the memory controller to provide the first set of access control signals to the memory at a first time and the second set of access control signals to the memory at a second time.

Fung disclose a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller (col. 1 lines 25-32, BIOS read on this limitation since the BIOS operates during a power up routine) for the purpose of determining a computer configuration thereby guaranteeing reliable operation of the system. Also it would have been readily appreciated by one of ordinary skill in the art that a system includes a power supply to provide a power to the system.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the power supply and a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller of Fung into the combined invention of Farrer, Micron, Wyland for the advantages stated above.

## *Conclusion*

12. The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

1. USP 5893136
2. USP 5721860
3. USP 5630163
4. USP 5604880
5. USP 5568651
6. USP 5325513
7. USP 5307320
8. USP 5278801
9. USP 5261064
10. USP 5253357
11. USP 5708791
12. USP 5701438
13. Micron, "Reduce DRAM cycle times with extended data-out", Micron technical Note pp 5-33 thru 5-40, 4/94.
14. Kristina Sullivan, "Simcheck add-on lets users identify faulty DRAM chips", PC week, May 7 1990, v7 n18 p18(1).
15. Old SIMCHECK Product Line, [Online] Available: http://www.simcheck.com/sim1pl.htm.

13. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

14. Applicants are requested to number each line of each claim starting with line number one to provide easier communication in the future.

15. When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to

locate the appropriate paragraphs.

16. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

17. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Do Yoo, can be reached on (703) 308-4908.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

18. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

**or faxed to:**

(703) 308-9051-2, (for formal communications intended for entry)

**Or:**

(703) 305-9731 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Patent Examiner
December 27, 2000